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Applications of Vedic Mathematics in Computer Arithmetic

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Abstract- Vedic mathematics or ancient mathematics is a unique technique of calculations based on 16 sutras. It provides an innovative way of computation of almost all the mathematical operations. In this era of digitization, engineers are working on increase speed of the digital circuits while reducing the size and power consumed. Vedic math reduces the computational steps required to achieve the result.

Keywords: Computer Arithmetic, Vedic Mathematics

Introduction : The simplicity in the VM is that the designs may be performed intellectually and further there have been many blessings of the usage of intellectual system. There are sixteen different Sutras in Vedic arithmetic that all may be implemented to several departments like geometry, algebra and trigonometry. Further, Sanskrit word "VEDA" is derived from the word "VID", because of this that to realize without limit. It primarily based totally at the sixteen sutras which offers with numerous fields of arithmetic inclusive of algebra, geometry, calculus, and more. The Vedic math's converts complicated calculations into smooth calculations.

Multiplier: The three vital approaches of multiplication are creating, lowering and eventually including the Partial product. If a multiplier needs to be green, it ought to have functions like Accuracy, fast performance, and strength green system & need to occupy few wide varieties of slices. Based on time taken and place consumed, the developments of multipliers are divided into three classes: The Serial multiplier, Parallel Multiplier & Serial Parallel Multiplier. The first stresses at the premiere utilization of the hardware particularly the chip place. The 2nd does fast mathematical operations and the 0.33 is a transaction among the primary classes.

Conversion Method of Binary number to Decimal number: This precise numbering approach entails the upward push of values from proper to left digits via way of means of fantastic integer powers beginning from 0 at the gadgets location raised at the common base of two. By neglecting the

corresponding virtual fee of binary digit fee zero and including the corresponding virtual fee of binary digit fee 1 the decimal quantity may be obtained. Convert binary quantity 10011101 into decimal quantity equivalent:

Decimal Digit Value	2^7 128	2^6 64	2^5 32	2^4 16	2^3 8	2^2 4	2^1 2	2^0 1
Binary Digit Value	1	0	0	1	1	1	0	1

Table 1: Binary number to Decimal number

Vedic Sūtras: computer applications: In maximum DSP processor multiplier is one essential a part of hardware due to that velocity of processor increases. "Finite Impulse Response filters typically known as the convolution filter consists of a multiplier involved in it. Execution of FFT wishes massive no. of multiplications & additions and due to that it turns into very complicated. So it's miles important to have excessive velocity and electricity ingesting multiplier to make it easy and rapid. To triumph over the above desires VM Sūtras are very helpful. VM Sūtras are carried out in decimal quantity gadget in addition to binary quantity gadget additionally. In this bankruptcy Vertically & Crosswise Sūtra primarily based totally multiplier for all sorts of multiplication, Nikhilaṁ Sūtra primarily based totally multiplier for the unique form of multiplication, Ekanyūnena Pūrveṁa Vedic Multiplier and Ānurūpyeṁa Sub-Sūtra primarily based totally multiplier for unique form of multiplication growth the modularity at the same time as lowering complexity of the layout required to enter larger bit numbers. Binary department through Nikhila approach for the numbers that are close to base 10 in addition extra simplifying the trouble and lowering the quantity of elements. Parāvartya Yojayet Sūtra as in opposition to Nikhila Sūtra for supporting in fixing larger issues of binary department, Dhwajaka a popular approach relevant to all form of binary department. Squaring through Dwandwayoga approach Duplex for a multiplication of quantity through itself (i.e. for squaring) & additionally Yāvadūnam Tāvadunī Krtya Vargañaca Yojayet Sub-Sūtra for squaring and cubing structure and Ānurūpyea Sub-Sūtra for cubing are mentioned through the researcher. Vedic Multiplier, Vedic Squaring and Cubing structure are the maximum green multiplier output referring to space, much less electricity consumption & rapidity than the traditional multipliers like Sequential, Booth, Array, Wallace Tree and Combinational multipliers.

Architecture of Vedic multiplier by Vertically & Crosswise Sūtra:

Vertically & Crosswise Sūtra primarily based on "Vedic multiplier" is relevant for the multiplication and exhibits performance of lowering the N × N bit multiplier to 2 × 2 bit shape.

The N × N bit multiplier shape is carried out via way of means of N × N gates and N 1/2 of adders and

(N-2)*N Full adder i.e. total (N-1) * N adders.

The 2 × 2 multiplier is carried out via way of means of four enter AND gates and a pair of 1/2 of adders. The four × four multiplier is carried out via way of means of sixteen enter AND gates four 1/2 of adders and eight complete adders. An eight × eight - bit multiplier is carried out via way of means of four four × four -bit multipliers and Three sixteen × sixteen bit adders.

With the assist of the fundamental 2 × 2 bit multiplier, multiplier with four via way of means of four bit developed, with the assist of four × four bit block, eight via way of means of eight bit block, sixteen via way of means of sixteen bit multiplier after which eventually 32 via way of means of 32 bit multiplier primarily based totally on Vedic Sūtra has been designed and consequently ALU layout with Vedic overlay set of rules is green associated with rapidity, location and energy consumption.

Binary Multiplication of 2 x 2 bit: (By using Vertically & Crosswise Sūtra based Vedic Multiplier).

Let C = C_1 C_0 and D = D_1 D_0 are assumed two bit nos. For conclusion C × D**,** It can be explained by figure 6.1 using Vertically & Crosswise Sūtra:

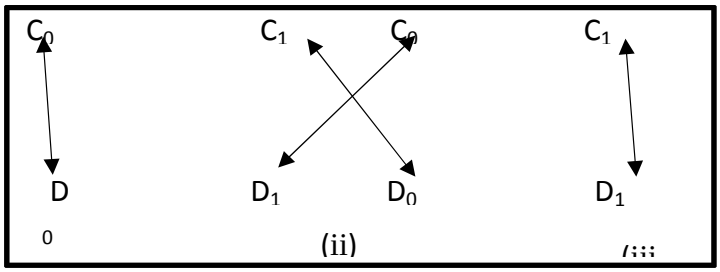

Figure 1: Vertically & Crosswise Sūtra

Performance Analyses of Vedic Algorithms

Table 2: Comparisons of various architecture utilizing Vedic and conventional way

S. No.	Implemented in	Conventional bits		Vedic bits	
		8	16	8	16
1	VLSI Application of High Presentation RSA Algorithm	30.25	56.96	25.12	53.89
2	High Speed Vigor Efficient ALU Design	30.01	47.82	14.39	23.59

3	Efficient Technique of Elliptic Arch Encryption	31.36	61.65	16.20	20.59
4	Efficient Technique of Elliptic Arch Encryption	612.87	1330.81	531.29	1310.5

Conclusion: Various parameters are endorsed via way of means of researchers to assess the overall performance of Vedic Math's algorithm. Researchers cautioned many parameters few of them are: Time, Delay, Power and Number of slices. The evaluation of Delay (ns) aspect for multiplication applied in special algorithms among Conventional and Vedic manner is proven in above Table.

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